Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method of protecting an integrated circuit from over voltage, the method comprising:

accepting a voltage from a power supply input to the integrated circuit;

accepting a pad voltage from an external voltage source;

comparing the power supply voltage to a predetermined value;

coupling a bias voltage for the integrated circuit to a gate of a PMOS (P-channel Metal Oxide Semiconductor) device when the power supply is below the predetermined value; and

coupling the pad voltage to a bias_mid node through the PMOS device to provide the bias voltage for the integrated circuit when the power supply is below the predetermined value.

2. (Currently Amended) ~~A method as in claim 1~~ A method of protecting an integrated circuit from over voltage, the method comprising:

accepting a voltage from a power supply input to the integrated circuit;

accepting a pad voltage from an external voltage source;

comparing the power supply voltage to a predetermined value;

coupling a bias voltage for the integrated circuit to a gate of a PMOS (P-channel Metal Oxide Semiconductor) device when the power supply is below the predetermined value; and

coupling the pad voltage to a bias_mid node through the PMOS device to provide the bias voltage for the integrated circuit when the power supply is below the predetermined value,

wherein coupling the bias voltage for the integrated circuit to the gate of the PMOS (P-channel Metal Oxide Semiconductor) device when the power supply is below the predetermined value comprises coupling the bias voltage to the gate of the PMOS (P-channel Metal Oxide Semiconductor) device through a first plurality of diode connected MOS devices when the power supply is below the predetermined value.

3. (Previously Presented) A method as in claim 1 wherein coupling the pad voltage to the bias_mid node through the PMOS device to provide the bias voltage for the integrated circuit further comprises using the source voltage of the PMOS device to couple the pad voltage to the bias_mid node.

4. (Previously Presented) A method of protecting an integrated circuit from over voltage, the method comprising:

accepting a voltage from a power supply input to the integrated circuit;

accepting a pad voltage from an external voltage source;

comparing the power supply voltage to a predetermined value;

coupling a bias voltage for the integrated circuit to a gate of a PMOS (P-channel Metal Oxide Semiconductor) device when the power supply is below the predetermined value; and

providing the pad voltage to an input of a plurality of diode connected MOS devices; and

coupling an output of the plurality of diode connected MOS devices to the drain of the PMOS device to couple the pad voltage to a bias_mid node to provide the bias voltage for the integrated circuit when the power supply is below the predetermined value.

5. (Previously Presented) A method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present the method comprising:

providing V_{DDO} to a gate of a first semiconductor device;

providing bias_mid to a source of the first semiconductor device such that the first semiconductor device will turn off when V_{DDO} - bias_mid is less than the threshold of the first semiconductor device; and

providing bias_mid to a gate of a MOS device in response to the turn off of the first semiconductor device to turn on the MOS device to couple Vpad to bias_mid.

6. (Previously Presented) The method of claim 5 wherein providing bias_mid to the gate of the MOS device in response to the turn off of the first semiconductor device to turn on the MOS device to couple Vpad to bias_mid comprises:

turning on a second semiconductor device and turning off a third semiconductor device which is coupled to the second semiconductor device thereby providing bias_mid to the gate of the MOS device to turn on the MOS device; and

using the turn on of the MOS device to couple Vpad to bias_mid.

Claims 7-22 (cancelled)

23. (Currently Amended) ~~The method of claim 6~~ A method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present the method comprising:

providing V_{DDO} to a gate of a first semiconductor device;

providing bias_mid to a source of the first semiconductor device such that the first semiconductor device will turn off when V_{DDO} - bias_mid is less than the threshold of the first semiconductor device; and

providing bias_mid to a gate of a MOS device in response to the turn off of the first semiconductor device to turn on the MOS device to couple Vpad to bias_mid,

wherein providing bias_mid to the gate of the MOS device in response to the turn off of the first semiconductor device to turn on the MOS device to couple Vpad to bias_mid comprises:

turning on a second semiconductor device and turning off a third semiconductor device which is coupled to the second semiconductor device thereby providing bias_mid to the gate of the MOS device to turn on the MOS device; and

using the turn on of the MOS device to couple Vpad to bias_mid, and

wherein using the turn on of the MOS device to couple Vpad to bias_mid comprises:

providing the pad voltage to an input of a first plurality of diode connected MOS devices; and

coupling an output of the first plurality of diode connected MOS devices to the drain of the MOS device.

24. (Currently amended) ~~The method of claim 5~~ A method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present the method comprising:

providing V_{DDO} to a gate of a first semiconductor device;

providing bias_mid to a source of the first semiconductor device such that the first semiconductor device will turn off when V_{DDO} - bias_mid is less than the threshold of the first semiconductor device; and

providing bias_mid to a gate of a MOS device in response to the turn off of the first semiconductor device to turn on the MOS device to couple Vpad to bias_mid,

wherein providing bias_mid to the gate of the MOS device comprises providing bias_mid to the gate of the MOS device through a second plurality of diode connected MOS devices in response to the turn off of the first semiconductor device.

25. (Currently Amended) ~~The method of claim 6~~A method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present the method comprising:

providing V_{DDO} to a gate of a first semiconductor device;

providing bias_mid to a source of the first semiconductor device such that the first semiconductor device will turn off when V_{DDO} - bias_mid is less than the threshold of the first semiconductor device; and

providing bias_mid to a gate of a MOS device in response to the turn off of the first semiconductor device to turn on the MOS device to couple Vpad to bias_mid,

wherein providing bias_mid to the gate of the MOS device in response to the turn off of the first semiconductor device to turn on the MOS device to couple Vpad to bias_mid comprises:

turning on a second semiconductor device and turning off a third semiconductor device which is coupled to the second

semiconductor device thereby providing bias_mid to the gate of the MOS device to turn on the MOS device; and

using the turn on of the MOS device to couple Vpad to bias_mid, and

wherein turning on a second semiconductor device and turning off a third semiconductor device comprises turning on a second semiconductor device, coupling Vpad to a gate of the third semiconductor device through a third plurality of diode connected MOS devices and the second semiconductor device to turn off the third semiconductor device.

26. (Currently Amended) The method of claim 4 further comprising:

providing V_{DDO} to a gate of a first semiconductor device

providing [~~a~~] the bias voltage for the integrated circuit to a source of the first semiconductor device such that the first semiconductor device will turn off when V_{DDO} minus the bias voltage for the integrated circuit is less than the threshold of the first semiconductor device; and

providing [~~a~~] the bias voltage for the integrated circuit to the PMOS (P-channel Metal Oxide Semiconductor) device in response to the turn off of the first semiconductor device to couple the pad voltage to a bias_mid node to provide the bias voltage for the integrated circuit when the power supply is below the predetermined value.

27. (Previously Presented) The method of claim 4 wherein providing the bias voltage for the integrated circuit to the gate of the PMOS (P-channel Metal Oxide Semiconductor) device in

response to the turn off of the first semiconductor device to couple the pad voltage to a bias_mid node comprises:

turning on a second semiconductor device and turning off a third semiconductor device which is coupled to the second semiconductor device thereby providing the bias voltage for the integrated circuit to the gate of the PMOS (P-channel Metal Oxide Semiconductor) device to turn on the PMOS (P-channel Metal Oxide Semiconductor) device; and

using the turn on of the PMOS (P-channel Metal Oxide Semiconductor) device to couple the pad voltage to a bias_mid node comprises.

28. (Previously Presented) The method of claim 4 wherein providing the bias voltage for the integrated circuit to the gate of the PMOS (P-channel Metal Oxide Semiconductor) device comprises providing the bias voltage for the integrated circuit to the gate of the PMOS (P-channel Metal Oxide Semiconductor) through a second plurality of diode connected MOS devices in response to the turn off of the first semiconductor device.

29. (Currently Amended) The method of ~~claim 11~~ claim 27 wherein turning on a second semiconductor device and turning off a third semiconductor device comprises turning on a second semiconductor device, coupling the bias voltage for the integrated circuit to a gate of the third semiconductor device through a third plurality of diode connected MOS devices and the second semiconductor device to turn off the third semiconductor device.

Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 17. This sheet, which includes Fig. 17, replaces the original sheet including Fig. 17. A redlined copy of Fig. 17 is also enclosed herewith.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes